DPDK SUMMIT
SAN FRANCISCO 2015

WELCOME TO DPDK SUMMIT SAN FRANCISCO 2015

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DPDK
DATA PLANE DEVELOPMENT KIT

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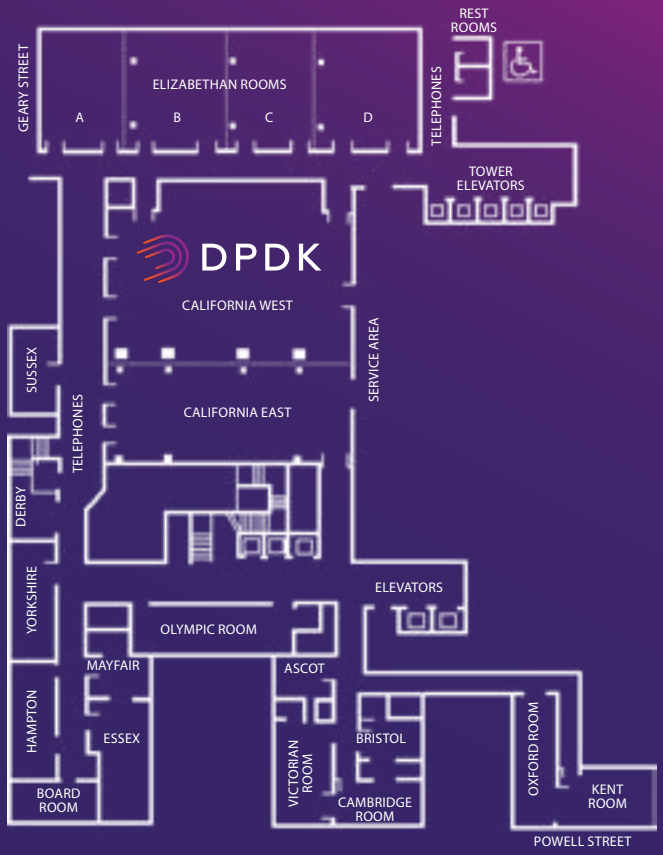
LOCATION MAP



AGENDA

General Sessions | California West

8:00 am - 8:45 am
Registration and Breakfast

8:45 am – 9:00 am
Opening Remarks and Kickoff to DPDK Summit
Tim O'Driscoll, Engineering Manager, Intel

9:00 am – 10:00 am
Leveraging DPDK to Scale-Out Network Functions Without Sacrificing Networking Performance
Tim Mortsolf, Chief Technology Officer
Scott Myelle, VP Solutions Architecture

RIFT.io

NFV application workloads are deployed in ecosystems with varying network attachment conditions that determine the availability of specific DPDK technologies. DPDK technology has rapidly evolved to support multiple I/O models ranging from dedicated access with PCI pass-through, shared access with SR-IOV, and vhost-user offload using a DPDK enabled Open vSwitch. This presentation demonstrates how to write a flexible network function that can utilize DPDK to its full potential while retaining the ability to run in a non-DPDK environment.

10:00 am - 10:15 am
Break/Networking

10:15 am – 11:15 am

Aspera's FASP Protocol Uses Standard Hardware and DPDK to Achieve 80Gbps Data Transfer

Charles Shiflett, Senior Software Engineer

IBM Aspera Solutions

Charles Shiflett will review the technologies and design approach to send data at a rate in excess of 1 TB every two minutes. Aspera Fast, Adaptive, and Secure Protocol (FASP®) is a breakthrough transfer protocol that leverages existing WAN infrastructure and commodity hardware. Code samples showing the use of DPDK, AES-NI, FASP Sockets, and direct I/O to create a zero-copy transfer technology will be discussed.

11:15 am – 12:15 pm

Future Enhancements to the DPDK Framework

Keith Wiles, Intel Architect

Intel

This session will provide insight and gather community input on forward-looking activity in advancing DPDK to include connectivity to hardware accelerators and SOC support. Keith will review the need for additional devices and functionality within the DPDK framework including supporting non-PCI configuration, external memory manager and event programming model utilized by many SOCs. The session will drill down on the use of a crypto device within the DPDK framework by reviewing an early proof of concept of a software and hardware implementation of the device.

12:15 pm – 1:00 pm

Networking Lunch

1:00 pm – 2:00 pm

It's kind of fun to do the impossible with DPDK

Yoshihiro Nakajima, Researcher

NTT Network Innovation Laboratories

NTT Network Innovation Laboratories will present lessons learned from a one year experiment on SDN/OpenFlow Lagopus Switch development and trials on ShowNet SDN-IX from Interop Tokyo 2015. A co-design of FPGA NIC, DPDK library extension and software data plane is indispensable to improve packet lookup/processing performance and to reduce CPU resources for 100Gbps packet processing performance. Additionly, NTT will share a carrier use case activity on hybrid SDN with autonomous network control and network policy control by their Lagopus switch and OpenFlow technologies.

2:00 pm – 3:00 pm

Design Considerations for a High-Performing Virtualized LTE Core Infrastructure

Arun Rajagopal, Chief Technology Officer, Sprint

Sameh Gobriel, Research Scientist, Intel

Sprint

Sprint's expectation is to achieve similar performance in moving from purpose built ASIC based platforms to virtualized network solutions running on high volume servers. This session will discuss the technical challenges in achieving a scalable solution that addresses the required transaction rates and throughput of a carrier network. Learn how DPDK, VM to VM communication optimizations, and cluster scaling technologies work together to create a scalable LTE core infrastructure built on high volume servers.

3:00 pm – 3:15 pm
Break/Networking

3:15 pm – 4:15 pm
Evaluation and Characterization of NFV Infrastructure Solutions on Hewlett-Packard Server Platforms
Al Sanders, Lead Developer

Hewlett-Packard
The HP Servers NFV Infrastructure Lab was formed to evaluate DPDK based environments to ensure that HP Server Platforms can provide the best possible performance for hosting NFV Solutions. The lab has partnered with a number of NFV providers, including Intel's Open Network Platform and 6WIND. Our testing methodology will be presented with a focus on packet processing throughput and latency in a variety of DPDK enabled configurations, including bare metal, SR-IOV, and accelerated virtual switches. Examples of results using Intel's ONP and 6WIND technologies will be presented.

4:15 pm – 5:15 pm
Open Discussion Panel (Q&A with Speakers)
Moderator: Jim St. Leger, Software Product Line Manger, Intel

5:15 pm – 5:30 pm
Closing Remarks

5:30 pm – 7:30 pm
Evening Reception
Imperial Floor (32nd Floor of Tower Building)

SPEAKERS

TIM O'DRISCOLL
Engineering Manager, Intel

Tim is a software engineering and program manager overseeing the DPDK project and development activities at Intel. He has a strong telecom background having spent his career working at Ericsson and Motorola in positions including engineering and system and solution architecture before coming to Intel. He's originally from Ireland and has traveled extensively including multiple posts around the globe.

TIM MORTSOLF
CTO and Co-Founder, RIFT.io

Tim Mortsolf is a co-founder and the chief technology officer of RIFT.io. As CTO, Mortsolf helps define the company's technology strategy and works directly with the engineering team to develop innovative product solutions. Mortsolf worked in software research and development fields of internet routing and subscriber management throughout his career at Bell Laboratories, U.S. Robotics, RedBack Networks and Starent Networks. Mortsolf co-founded and served as the chief architect at Affirmed Networks. Mortsolf holds a large number of issued patents in the telecommunications and internet technology fields and is an author of several Internet Engineering Task Force (IETF) networking standards. At U.S. Robotics, Mortsolf defined the Point-to-Point Tunneling Protocol

(PPTP) that enables secure remote access to corporate networks across the public Internet. For his work in this field, he was a recipient of the PC Magazine Networking Software Innovation of the Year award. Mortsolf is a summa cum laude graduate from the University of Massachusetts and holds several degrees in physics, chemistry, as well as biochemistry and molecular biology.

SCOTT MYELLE

VP Solutions Architecture, RIFT.io

Scott Myelle is a 20 year communication industry veteran with experience creating solutions and implementing them. At RIFT.io he has responsibility for Solution Architecture, working closely with customers to evangelize RIFT.io's vision and understand their future needs and requirements. Throughout his career Scott's passion has been on evolving networking architectures from the days of TDM through the most modern cloud designs. Prior to RIFT.io Scott managed a group of Consulting Solution Architects at Cisco System focused on the intersection of cloud, virtualization and software defined networking. Prior to Cisco, Scott held several management positions at Contextream (acquired by HP), Tellabs and United Pan-Europe Communications (acquired by Liberty Global).

CHARLES SHIFLETT

Senior Software Engineer, IBM Aspera Solutions

Charles Shiflett is a senior software engineer at Aspera, an IBM company. Shiflett works as the lead developer and architect for Aspera's Next Generation FASP. Next Generation FASP is a high speed (80Gbps), adaptive, secure and reliable congestion controlled transfer protocol built upon Aspera's FASP transfer protocol. Shiflett has a Bachelor of Science in computer engineering from UC Santa Cruz, and a slight obsession with improving transfer I/O.

KEITH WILES

Staff Architect, Intel Corporation

Keith Wiles is a staff architect at Intel Corporation working with DPDK and NFV acceleration technologies for accelerated networking performance. Wiles serves as a contributing member in the Data Plane Acceleration group (DPACC) within OPNFV. Wiles also authored Pktgen-DPDK, a network traffic generator running on DPDK. He wrote Pktgen-DPDK while working at Wind River to understand DPDK and introduce DPDK as part of the network acceleration platform products within Wind River. He worked at Wind River for 16 years while enhancing VxWorks Real Time networking stack. Wiles designed and wrote the CertStack a DO-178B certified TCP/IPv4 network stack used in the MILS and AIRINC platforms. Wiles was also a founding member, chief technology officer and chief financial officer of XAct Inc before Wind River acquired the company that produced

software and hardware for Ethernet managed and unmanaged switch designs.

YOSHIHIRO NAKAJIMA

Researcher, NTT Network Innovation Laboratories

Yoshihiro Nakajima received his Bachelor of Science in information science in 2003, a Master of Engineering degree in 2005, and the doctorate degree in computer science in 2008 from the University of Tsukuba. He worked as a research fellow at the Japan Society for the Promotion of Science from 2005 to 2008. He joined NTT Network Innovation Laboratories in 2008 and studied high-performance stream processing systems and a multi-layer network management system. He is a project lead for a high-performance SDN/OpenFlow switch called Lagopus vSwitch. His interests include high-performance software packet processing middleware and technologies. He is a member of the Association for Computing Machinery (ACM) and Institute of Electrical and Electronics Engineers (IEEE).

ARUN RAJAGOPAL

Technology Architect, NFV and Wireless Core, Sprint

Arun Rajagopal works in the chief technology officer's office at Sprint and manages technology strategy and architecture for NFV. In his current role, he defines the long term architecture for NFV, develops architecture evolution plans and creates requirements for NFV adoption at Sprint. This includes looking at global mobile technology requirements and trends and creating strategies for adoption or adaption to meet Sprint's needs over the medium to long term. Prior to working at Sprint, Rajogopal was the chief network architect at Reliance Globalcom and responsible for strategy, architecture and design for Reliance's global IP network that spans over 200 countries. Rajagopal has a Bachelor of Technology in electronics and communications engineering from Calicut University in India and a Master of Computer Engineering from Texas A&M University.

SAMEH GOBRIEL

Senior Research Scientist, Intel Labs

Sameh Gobriel is a senior research scientist at Intel Labs where he drives research to enable future products to be best-in-class in energy-efficient performance. His research interests include platform I/O architecture, software networking, Network Functions Virtualization and energy-efficient design of computer platforms.

He received his BE in Electronics and Electrical Communications Engineering from Cairo University in 1999, the MS and the PhD degree in computer science from the University of Pittsburgh in 2007 and 2008, respectively.

Dr. Gobriel is the author of more than 30 research papers, articles and book chapter in first tier conferences and journals; he has 28 filed technology patents. For his outstanding research work at Intel Labs he has received a few career awards including an Intel Achievement Award for

his research on Energy-Efficient WiFi Interfaces. He has served on the program committees of numerous conferences and workshops.

AL SANDERS

Lead Developer, Hewlett-Packard

Al Sanders works in part with the Hewlett-Packard (HP) Server Telco team managing the NFV Infrastructure Lab. The lab partners with NFV technology providers to ensure that HP Server platforms provide optimal NFV Infrastructure and packet processing performance. Sanders worked at HP for 33 years and worked on Linux solutions for Telco customers for the past 8 years. Previous assignments include work on HP-UX kernel drivers, DCE RPC and DFS environments as well as hardware simulation tools. Sanders graduated from the Massachusetts Institute of Technology in 1982 with a Bachelor and Master of Computer Science.

JIM ST. LEGER

Software Product Line Manager
Intel® Network Platforms Group

Jim St. Leger is a software product line manager in Intel's Network Platforms Group. His work includes software that accelerates network traffic and applications as well as improving the speed and efficiency of packet-based networks through the use of multicore processors and software technologies.

Prior to Intel, St. Leger worked in various manufacturing, product engineering and marketing roles in the automotive, aerospace and semiconductor equipment industries. He holds a Bachelor of Science in mechanical engineering from Rensselaer Polytechnic Institute (a.k.a. RPI) and a Master of Management in manufacturing (MMM) from Northwestern University (McCormick School of Engineering & Kellogg School of Management.)

St. Leger spends his off-hours focused on his family, the outdoors, lifelong learning and a myriad of other random pursuits. He works as an advisory board member to Hacking Autism, mentors a local FIRST Robotics team and chairs the KAET Arizona PBS Community Advisory Board. Follow him on Twitter: @Intel_Jim.

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